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10/757,222	01/14/2004	John David Kaewell JR.	1-1-0064.5US	3792

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EXAMINER

CHEN, JUNPENG

ART UNIT	PAPER NUMBER
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2618

MAIL DATE	DELIVERY MODE
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05/13/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

1. This action is in response to applicant's amendment/arguments filed on 10/09/2007. Claims 9, 14, 16, 19, 24, 26, 34, 36 and 29 have been amended. Claims 13, 17, 23, 27, 33 and 37 have been canceled. Currently, claims 9-12, 14-16, 18-22, 24-26, 28-32, 34-36, 38 and 39 are pending. **This action is made FINAL.**

Information Disclosure Statement

2. The information disclosure statement submitted on 11/13/2008 and 12/22/2008 have been considered by the Examiner and made of record in the application file.

Response to Arguments

3. Applicant's arguments filed on 02/12/2009 have been fully considered but they are not persuasive.

Applicant argues that Wieczorek does not disclose three different power modes, namely, an on power consumption level mode, an off power consumption level mode, and at least one intermediate power consumption level mode. The Examiner respectfully disagrees. According to col. 5 with lines 4-23, Wieczorek discloses a low power mode (read as the at least one intermediate power consumption level mode), a non-energy saving mode (read as the on power consumption level mode). In addition, when the communicate device is turned off (powered off), it is in off power consumption level mode. Therefore, Wieczorek discloses three different power modes.

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Applicant further argues that Wieczorek does not disclose wherein one of the plurality of circuit components transitions between at least two power consumption levels during any single time slot. The Examiner respectfully disagrees. According to col. 5 with lines 4-23, Wieczorek discloses that the communication device may be deactivated for a minimum of three quarters of a four slot TDM frame during low power mode, and the communication device operates to receive both of the preferably control slots during non-energy saving mode. Therefore, during a time slot, the communication device changes from low power mode to non-energy saving mode.

Response to Amendments

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Wieczorek et al. (U.S. Patent 5,150,361).

Consider **claim 9**, Wieczorek discloses a time division multiple access (TDMA) wireless subscriber unit comprising:

a plurality of circuit components configured to operate in a plurality of signal processing states, each of the plurality of signal processing states having an on power consumption level, an off power consumption level, and at least one intermediate

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power consumption level for at least one of the plurality of circuit components on a call state basis (read as the lower power mode, non-energy saving mode, and the off mode of the communication device, col. 5 with lines 4-21); and a power interface circuit coupled to the plurality of circuit components configured to provide the power consumption levels (read as battery saver 351, Figure 3); wherein at least one of the plurality of circuit components transitions among the plurality of signal processing states based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit (read as the D/A 322, col. 4 with lines 24-27).

Consider **claim 19**, Wieczorek discloses a method for use in a time division multiple access (TDMA) wireless subscriber unit, the method comprising: synchronizing phase with a received signal (read as the synchronization signal 310, controller 320 and synthesizer 334, Figure 3, col. 4 with lines 1-63); operating a plurality of circuit components according to a plurality of signal processing states, each of the plurality of signal processing states having an on power consumption level, an off power consumption level, and at least one intermediate power consumption level for at least one of the plurality of circuit components on a call state basis (read as the lower power mode, non-energy saving mode, and the off mode of the communication device, col. 5 with lines 4-21); transitioning at least one of the plurality of circuit components among the plurality of signal processing states based on a time slot of a TDMA frame assigned to the TDMA wireless subscriber unit (read as the D/A 322, col. 4 with lines 24-27).

Consider **claim 29**, Wieczorek discloses a processor comprising: a power interface circuit configured to power a plurality of circuit components that operate in a

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plurality of signal processing states, each of the plurality of signal processing states having an on power consumption level, an off power consumption level, and at least one intermediate power consumption level for at least one of the plurality of circuit components on a call state basis (read as the lower power mode, non-energy saving mode, and the off mode of the communication device, col. 5 with lines 4-21); wherein at least one of the plurality of circuit components transitions among the plurality of signal processing states based on a time slot of a TDMA frame (read as the D/A 322, col. 4 with lines 24-27).

Consider **claims 10, 20 and 30, as applied to claims 9, 19 and 29 above respectively**, Wieczorek discloses a plurality of clocks, wherein one of the plurality of clocks is selected for each of the plurality of circuit components based on a current one of the plurality of signal processing states (read as the various clock signals, including but not limited to a TDM frame clock, slot clock, and data symbol clock that also exist in the RF communication units in Figure 3, col. 2 with lines 60-57).

Consider **claims 11, 21 and 31, as applied to claim 10, 20 and 30 above respectively**, Wieczorek discloses wherein the plurality of clocks is produced by a software controlled register coupled to the plurality of circuit components (read as controller 320 inherently having software in it to process instructions to operate the communication unit, Figure 3, col. 4 with 39-66).

Consider **claims, 12, 22 and 32, as applied to claims 9, 19 and 29 above respectively**, Wieczorek discloses wherein at least one of the plurality of signal

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processing states includes a reduced power sub-state (read as, i.e. the controller greatly reduces the speed of its own operation, col. 4 with lines 57-60).

Consider **claims 14, 24 and 34, as applied to claims 13, 23 and 33 above respectively**, Wieczorek discloses wherein the at least one intermediate power consumption level includes retaining operating state information to resume processing in response to a transition to one of the plurality of signal processing states (read as the controller 320 maintains operating and reduces its speed of its operation during power saving mode, and fully operating to process the information in non-energy saving mode, col. 4 with lines 57-60).

Consider **claims 15, 25 and 35, as applied to claims 9, 19 and 29 above respectively**, Wieczorek discloses wherein at least one of the plurality of circuit components are selectively power down during a call connection (read transmitter 324 is deactivated unless the communication unit is transmitting, col. 4 with lines 24-30).

Consider **claims 16, 26 and 36, as applied to claims 9, 19 and 29 above respectively**, Wieczorek discloses wherein the plurality of circuit components are selectively powered responsive to a radio control channel timeslot to determine the presence of call traffic or a traffic channel assigned to the TDMA wireless subscriber unit (read as the re-activation of the circuit in the receiving section, col. 4 with line 60 to col. 5 with line 49).

Consider **claims 18, 28 and 38, as applied to claims 9, 19 and 29 above respectively**, Wieczorek discloses wherein one of the plurality of circuit components transitions between at least two power consumption levels during any single time slot

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(read as that the communication device may be deactivated for a minimum of three quarters of a four slot TDM frame during low power mode, and the communication device operates to receive both of the preferably control slots during non-energy saving mode. Therefore, during a time slot, the communication device changes from low power mode to non-energy saving mode, col. 5 with lines 4-17).

Consider **claim 39, as applied to claim 29 above**, Wieczorek discloses wherein at least one of the plurality of circuit components is collocated with the processor (read as Figure 3)

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any response to this Office Action should be **faxed to (571) 273-8300 or mailed to:**

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P.O. Box 1450
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Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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Junpeng Chen
J.C./jc

/Edward Urban/

Supervisory Patent Examiner, Art Unit 2618